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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,479	02/04/2004	Masaki Ito	NITT.0189	1890

7590 10/06/2004  
REED SMITH LLP  
Suite 1400  
3110 Fairview Park Drive  
Falls Church, VA 22042

EXAMINER
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THOMPSON, ANNETTE M

ART UNIT	PAPER NUMBER
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2825

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/770,479

Applicant(s)

ITO, MASAKI

Examiner

A. M. Thompson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 04 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 02/04/2004.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

This application, 10/770,479, has been examined. Claims 1-5 are pending.

#### ***Priority***

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 06/02/2001. It is noted, however, that applicant has not filed, either with the instant application or with the parent application a certified copy of the Japanese application as required by 35 U.S.C. 119(b).

#### ***Information Disclosure Statement***

2. The foreign patent document listed on Applicant's PTO-1449 has not been considered because it has not been provided with the Applicant's filing and a concise explanation of its relevance is not included.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Rejection of claims 1-5**

4. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Rajsuman et al. (Rajsuman), U.S. Patent 6,678,645. Rajsuman discloses a method and apparatus for SOC design validation.

5. Pursuant to claim 1, Rajsuman discloses a semiconductor integrated circuit device (Abstract, Figure 3) comprising first and second circuit blocks (Fig. 3, #41, A, B, C); an interface checker to monitor whether waveforms of signals between the first and second circuit blocks conform to an interface specification of a design data of the first circuit block (col. 5, ll. 16-30); and an external output pin to output a result of a monitoring of the interface checker to an external of the semiconductor IC device (Fig. 3).

6. Pursuant to claim 2 wherein the external output pin outputs a value indicating conformity or non-conformity (col. 7, ll. 60-65, the response comparison).

7. Pursuant to claim 3, wherein the interface specification describes timing information in synchronization with a clock signal (col. 10, ll. 4-40).

8. Pursuant to claim 4, Rajsuman discloses a method (Abstract) that provides design data and an interface specification of the design data; generates a synthesizable interface checker in accordance with the specification (col. 10, line 40 to col. 11, line 27); produces a semiconductor IC including a first logic circuit (col. 6, ll. 33-56); monitors whether waveforms of signals between circuit blocks conform to an interface specification. (col. 9, line 34 to col. 10, line 39, the verification unit).

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9. Pursuant to claim 5, further comprising outputting a first value indicating a conformity of the waveforms to the interface specification or a second value indicating a nonconformity of the waveforms to the interface specification to an external of the semiconductor IC (col. 7, ll. 60-65, the response comparison).

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please reference the PTO-892 for a listing of pertinent references.

11. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m..

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop \_\_\_\_\_

Commissioner for Patents


P.O. Box 1450

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or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)



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